

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	233	703/20.ccls.	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 13:35
L2	45	ebiu	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 13:52
L3	100	(bus adj interface adj unit) and soc and test\$3	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 14:10
L4	47	L3 and verif\$7	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 14:11
L5	25	L4 and @ad<"20020301"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 14:11
L6	7	(bus adj interface adj module) and soc and test\$3	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 14:14

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L9.	65	soc and verif\$7 and ((test adj bench) or testbench) and @ad<"20020301"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2008/02/27 14:45


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) | [Purchase History](#) |

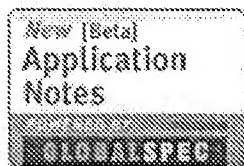
Welcome United States Patent and Trademark Office

[Search Results](#)[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "(ebiu) <and> (pyr >= 1913 <and> pyr <= 2002)"

Your search matched 5 of 1752210 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.



» Search Options

[View Session History](#)[New Search](#)

» Key

IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

Modify Search

(ebiu) <and> (pyr >= 1913 <and> pyr <= 2002)

[Search](#)☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract[IEEE/IET](#)[Books](#)[Educational Courses](#)[A](#)

IEEE/IET journals, transactions, letters, magazines, conference proceedings, and

[view selected items](#)[Select All](#) [Deselect All](#)

- ☐ 1. **Core design and system-on-a-chip integration**
 Rincon, A.M.; Cherichetti, G.; Monzel, J.A.; Stauffer, D.R.; Trick, M.T.;
[Design & Test of Computers, IEEE](#)
 Volume 14, Issue 4, Oct.-Dec. 1997 Page(s):26 - 35
 Digital Object Identifier 10.1109/54.632878
[AbstractPlus](#) | Full Text: [PDF](#)(228 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 2. **A Computer Vision and Robotics Laboratory**
 Jarvis, R.A.;
 Computer
 Volume 15, Issue 6, Jun 1982 Page(s):8 - 24
[AbstractPlus](#) | Full Text: [PDF](#)(11232 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 3. **A Stability Criterion for Linear Networks Containing Time-Varying Capac**
 Sandberg, I.;
[Circuits and Systems, IEEE Transactions on \[legacy, pre - 1988\]](#)
 Volume 12, Issue 1, Mar 1965 Page(s):2 - 11
[AbstractPlus](#) | Full Text: [PDF](#)(984 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 4. **Multirate and composite control of two-time-scale discrete-time systems**
 Litkouhi, B.; Khalil, H.;
[Automatic Control, IEEE Transactions on](#)
 Volume 30, Issue 7, Jul 1985 Page(s):645 - 651
[AbstractPlus](#) | Full Text: [PDF](#)(784 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 5. **An overview of the COBRA-ABS high level synthesis system for multi-FI**
 Duncan, A.A.; Hendry, D.C.; Gray, P.;
 FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE Symposium
 15-17 April 1998 Page(s):106 - 115
 Digital Object Identifier 10.1109/FPGA.1998.707888


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) | [Purchase History](#) |

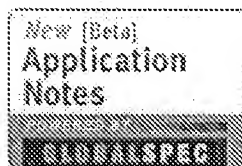
Welcome United States Patent and Trademark Office

[Search Results](#)[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "((soc<and>verif*)) <and> (pyr >= 1913 <and> pyr <= 2002)"

Your search matched 1118 of 1751101 documents.

A maximum of 500 results are displayed, 25 to a page, sorted by Relevance in Descending order.



Modify Search

((soc<and>verif*)) <and> (pyr >= 1913 <and> pyr <= 2002)

[Search](#)☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract

» Search Options

[View Session History](#)[New Search](#)[IEEE/IET](#)[Books](#)[Educational Courses](#)[A](#)

IEEE/IET journals, transactions, letters, magazines, conference proceedings, and

» Key

[view selected items](#)[Select All](#) [Deselect All](#)View: 1-25 | [26-50](#)

IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

- ☐ 1. **C-based SoC design flow and EDA tools: an ASIC and system vendor pe**
 Wakabayashi, K.; Okamoto, T.;
 Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction
 Volume 19, Issue 12, Dec. 2000 Page(s):1507 - 1522
 Digital Object Identifier 10.1109/43.898829
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(388 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 2. **Constraint driven pin mapping for concurrent SOC testing**
 Yu Huang; Nilanjan Mukherjee; Chien-Chung Tsai; Samman, O.; Yahya Zaid;
 Tung Cheng; Reddy, S.M.;
 Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th A:
 the 15th International Conference on VLSI Design. Proceedings.
 7-11 Jan. 2002 Page(s):511 - 516
 Digital Object Identifier 10.1109/ASPDAC.2002.994971
[AbstractPlus](#) | Full Text: [PDF](#)(413 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ 3. **RF-SoC-expectations and required conditions**
 Matsuzawa, A.;
 Microwave Theory and Techniques, IEEE Transactions on
 Volume 50, Issue 1, Part 2, Jan. 2002 Page(s):245 - 253
 Digital Object Identifier 10.1109/22.981277
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(402 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 4. **A battery management system for stand-alone photovoltaic energy syst**
 Duryea, S.; Islam, S.; Lawrance, W.;
 Industry Applications Magazine, IEEE
 Volume 7, Issue 3, May-June 2001 Page(s):67 - 72
 Digital Object Identifier 10.1109/2943.922452
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1256 KB) IEEE JNL
[Rights and Permissions](#)


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alerts](#) | [Purchase History](#) |

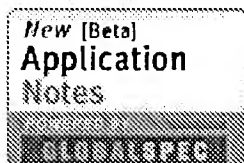
Welcome United States Patent and Trademark Office

[Search Results](#)[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "((soc<and>testbench)) <and> (pyr >= 1913 <and> pyr <= 2002))"

Your search matched 35 of 1752210 documents.

A maximum of 100 results are displayed, 25 to a page, sorted by Relevance in Descending order.



Modify Search

((soc<and>testbench)) <and> (pyr >= 1913 <and> pyr <= 2002)

[Search](#)☐ Check to search only within this results setDisplay Format: ☒ Citation ☐ Citation & Abstract

» Search Options

[View Session History](#)[New Search](#)[IEEE/IET](#)[Books](#)[Educational Courses](#)[A](#)

IEEE/IET journals, transactions, letters, magazines, conference proceedings, and

» Key

[view selected items](#)[Select All](#) [Deselect All](#)

IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

- ☐ 1. **EDA in IBM: past, present, and future**
 Darringer, J.; Davidson, E.; Hathaway, D.J.; Koenemann, B.; Lavin, M.; Morre Roesner, W.; Schanzenbach, E.; Tellez, G.; Trevillyan, L.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction Volume 19, Issue 12, Dec. 2000 Page(s):1476 - 1497
 Digital Object Identifier 10.1109/43.898827
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(320 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 2. **An industrial view of electronic design automation**
 MacMillen, D.; Camposano, R.; Hill, D.; Williams, T.W.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction Volume 19, Issue 12, Dec. 2000 Page(s):1428 - 1448
 Digital Object Identifier 10.1109/43.898825
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(180 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ 3. **System architecture for multi-technology testbench-on-a-chip**
 Hodge, A.; Newcomb, R.; Zaghloul, M.; Tigli, O.;
Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on Volume 2, 26-29 May 2002 Page(s):II-736 - II-739 vol.2
 Digital Object Identifier 10.1109/ISCAS.2002.1011458
[AbstractPlus](#) | Full Text: [PDF](#)(467 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ 4. **C-based SoC design flow and EDA tools: an ASIC and system vendor pe**
 Wakabayashi, K.; Okamoto, T.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction Volume 19, Issue 12, Dec. 2000 Page(s):1507 - 1522
 Digital Object Identifier 10.1109/43.898829
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(388 KB) IEEE JNL
[Rights and Permissions](#)

Test scheduling of BISTed memory cores for SoC


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)



Scholar [All articles](#) - [Recent articles](#) Results 1 - 10 of about **38,000** for soc verification. (0.25 sec)

All Results

[W Swann](#)
[W Hunt](#)
[K Albin](#)
[M Birnbaum](#)
[M Srivas](#)

Nuts and Bolts of Core and SoC Verification - all 11 versions »

K Albin - 38th Design Automation Conference (DAC'01), 2001 - doi.ieeecomputersociety.org

Nuts and Bolts of Core and **SoC Verification** ... 5. CONCLUSIONS The fundamental problem

that **SoC** and Core **verification** efforts deal with is design complexity. ...

Cited by 26 - Related Articles - Web Search

Verification of configurable processor cores - all 8 versions »

M Puig-Medina, G Ezer, P Konas - Proceedings of the Design Automation Conference (DAC2000), 2000 - doi.ieeecomputersociety.org

... Traditional processor **verification** environments cannot be easily merged into an **SOC verification** environment. In contrast, the ...

Cited by 18 - Related Articles - Web Search

IP reuse creation for system-on-a-chip design - all 3 versions »

PJ Bricaud - Custom Integrated Circuits, 1999. Proceedings of the IEEE ..., 1999 - ieeexplore.ieee.org

... creation for **SoC** design will be separated into system-level specification, soft-hard macro creation and productization, **SoC** integration and **SoC verification**. ...

Cited by 21 - Related Articles - Web Search

How VSIA answers the SOC dilemma - all 6 versions »

M Birnbaum, H Sachs - Computer, 1999 - ieeexplore.ieee.org

... Bus VCI and transaction specifications Implementation/**Verification** Phase 3: functional models for soft and hard virtual components, **SOC verification**, and firm ...

Cited by 55 - Related Articles - Web Search

Formal verification of the AAMP5 microprocessor - all 2 versions »

MK Srivas, SP Miller - Applications of Formal Methods, 1995 - citeseer.ist.psu.edu

... by: More Formal **verification** of the ARM6 micro-architecture - Fox (2002) (Correct)

Nuts and Bolts of Core and **SoC Verification** - Albin (2001) (Correct) Our ...

Cited by 39 - Related Articles - Cached - Web Search

Magic Numbers for Sphere Packings: Experimental Verification in Free Xenon Clusters - all 2 versions »

O Echt, K Sattler, E Recknagel - Physical Review Letters, 1981 - APS

... **Soc.** ... PHYSICAL REVIEW LETTERS Magic Numbers for Sphere Packings: Experimental

Verification in Free Xenon Clusters O. Echt, K. Sattler, and E. Recknagel Fakultdt ...

Cited by 323 - Related Articles - Web Search

[BOOK] System-On-A-Chip Verification: Methodology and Techniques - all 2 versions »

P Rashinkar, P Paterson, L Singh - 2001 - books.google.com

... 16 1.3.2 **SOC** Hardware RTL **Verification** 17 Page 7. vi **SOC Verification** 1 .3.3 **SOC** Software **Verification** 18 ... 85 Page 9. viii **SOC Verification** 3.3.4 ASB Master 86 ...

Cited by 82 - Related Articles - Web Search - Library Search


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

[Ad](#)
[Sc](#)
[Sc](#)
Scholar

 Results 1 - 4 of 4 for [ebiu soc verification](#). (0.15 seconds)

All Results

 Did you mean: [edu soc verification](#)
[A Rincon](#)
[G Cherichetti](#)
[J Monzel](#)
[D Stauffer](#)
[M Trick](#)
[An embedded PowerPC TM SOC for test and measurement applications](#)

 B Blaner, D Czenkusch, R Devins, S Stever - ASIC/SOC Conference, 2000. Proceedings 13th Annual IEEE , 2000 - [ieeexplore.ieee.org](#)

... to the HSMC, or SDRAM to SDRAM), between memory and an external peripheral attached

 to the **EBIU**, or between ... IV. DESIGN VERIFICATION The **SOC** was verified ...

 Cited by 3 - [Related Articles](#) - [Web Search](#)
[Core design and system-on-a-chip integration - all 7 versions »](#)

 AM Rincon, G Cherichetti, JA Monzel, DR Stauffer, ... - Design & Test of Computers, IEEE, 1997 - [ieeexplore.ieee.org](#)

 ... The PowerPC **EBIU** and code decompression cores connect ... are equally important to the

SOC designer, providing an ... by allowing de- sign and **verification** of macro ...

 Cited by 35 - [Related Articles](#) - [Web Search](#)
[Designer configurable multi-processor system - all 2 versions »](#)

 C Ussery, O Levia, J Gostomski, G Derti, MA ... - 2001 - [freepatentsonline.com](#)

 ... Unit (IBIU) or External Bus Interface Unit (**EBIU**). ... code generator 290 can also generate **verification** code 302 ... suited for System on Chip (**SoC**) architectures an ...

 Cached - [Web Search](#)
[An Overview of the COBRA-ABS High Level Synthesis System for Multi-FPGA Systems - all 5 versions »](#)

 AA Duncan, DC Hendry, P Gray - Proc. Field-Programmable Custom Computing Machines, April, 1998 - [doi.ieeecomputersociety.org](#)

 ... (**EBIU**) Data Only External Bus Interface Unit ... on emerging "system-on-chip" (**SOC**) devices

 incorporating ... Upon successful **verification**, the be- havioural layer ...

 Cited by 22 - [Related Articles](#) - [Web Search](#)

 Did you mean to search for: [edu soc verification](#)

[Google Home](#) - [About Google](#) - [About Google Scholar](#)


[Web](#) [Images](#) [Video](#) [News](#) [Maps](#) [more »](#)

Scholar

 Results 1 - 8 of 8 for **ebiu soc** . (0.07 seconds)

All Results

 Did you mean: **edu soc**
[A Rincon](#)
[A Duncan](#)
[G Cherichetti](#)
[J Monzel](#)
[D Stauffer](#)

An embedded PowerPC TM SOC for test and measurement applications
 B Blaner, D Czenkusch, R Devins, S Stever - ASIC/SOC Conference, 2000. Proceedings
 13th Annual IEEE ... , 2000 - [ieeexplore.ieee.org](#)
 ... to SDRAM), between memory and an external peripheral attached to the **EBIU**, or
 between ...
 Almost all cores on the **SOC** have some form of power management, ranging ...
 Cited by 3 - Related Articles - Web Search

Target directed completion for bus transactions

 BC Drerup, RN Iachetta Jr - 2002 - [freepatentsonline.com](#)

... 1, **SOC** 100 further comprises a target directed completion device 103 for providing
 an enhanced bus transaction interface between **EBIU** device 120, processor ...

Cached - Web Search

Core design and system-on-a-chip integration - all 7 versions »

 AM Rincon, G Cherichetti, JA Monzel, DR Stauffer, ... - Design & Test of Computers, IEEE,
 1997 - [ieeexplore.ieee.org](#)

... The PowerPC **EBIU** and code decompression cores connect directly to the PLB bus ...
 These

toolkits are equally important to the **SOC** designer, providing an efficient ...

Cited by 35 - Related Articles - Web Search

An Overview of the COBRA-ABS High Level Synthesis System for Multi-FPGA Systems - all 5 versions »

 AA Duncan, DC Hendry, P Gray - Proc. Field-Programmable Custom Computing Machines,
 April, 1998 - [doi.ieeeecomputersociety.org](#)

... (**EBIU**) Data Only External Bus Interface Unit ... at board level, as a multi-chip mod-
 ule (MCM), or on emerging "system-on-chip" (**SOC**) devices incorporating ...

Cited by 22 - Related Articles - Web Search

On the discretization of differential and Volterra integral equations with variable delay - all 3 versions »

H Brunner - BIT Numerical Mathematics, 1997 - Springer

... Thus, at the mesh point $t = t_{n+1}$ the value of u is $m_{bh} m_{uit}(t, +1) =$
 $ah \text{ Ebiu}_{,,i} + q \text{ E \&i('),uq,,i j=l j=l + Yo + au(s) ds + q ...}$

Cited by 18 - Related Articles - Web Search

Designer configurable multi-processor system - all 2 versions »

 C Ussery, O Levia, J Gostomski, G Derti, MA ... - 2001 - [freepatentsonline.com](#)

... as an Internal Bus Interface Unit (IBIU) or External Bus Interface Unit (**EBIU**). ... the
 present invention are well suited for System on Chip (**SoC**) architectures an ...

Cached - Web Search

Scattering of stable and unstable waves in a flow duct - all 11 versions »

B Nilsson - The Quarterly Journal of Mechanics and Applied Mathematics, 1998 - Oxford